

**This Page Is Inserted by IFW Operations  
and is not a part of the Official Record**

## **BEST AVAILABLE IMAGES**

**Defective images within this document are accurate representations of the original documents submitted by the applicant.**

**Defects in the images may include (but are not limited to):**

- **BLACK BORDERS**
- **TEXT CUT OFF AT TOP, BOTTOM OR SIDES**
- **FADED TEXT**
- **ILLEGIBLE TEXT**
- **SKEWED/SLANTED IMAGES**
- **COLORED PHOTOS**
- **BLACK OR VERY BLACK AND WHITE DARK PHOTOS**
- **GRAY SCALE DOCUMENTS**

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

We Claim:

## 1. An integrated circuit, comprising:

electrical connecting elements each having one of a first conductivity state and a second conductivity state different from said first conductivity state, said first and second conductivity states being brought about by impressing energy;

a substrate having a substrate surface with a first extension direction and a second extension direction running perpendicular to said first extension direction;

first and second connecting elements of said electrical connecting elements, as seen in said second extension direction, being disposed next to one another above said substrate surface in a first wiring plane, said first connecting element having an end, said second connecting element having an end;

third and fourth connecting elements of said electrical connecting elements, as substantially seen in said second extension direction, being disposed next to one another on said substrate surface, said third electrical connecting element having an end, said fourth electrical connecting element having an end, said ends of said third and fourth connecting elements being spaced apart along said first

extension direction from said ends of said first and second electrical connecting elements;

said first electrical connecting element, as seen in said second direction, being at a first distance from said second electrical connecting element;

a first interconnect:

being disposed above said substrate surface;

being connected to said first electrical connecting element; and

being disposed in said first wiring plane;

a second interconnect:

being disposed above said substrate surface;

being connected to said second electrical connecting element; and

being disposed at least partly in a second wiring plane located nearer to said substrate surface than said first wiring plane; and

said first and said second interconnects:

being disposed between said third and fourth electrical connecting elements; and

defining a second distance therebetween smaller than said first distance.

2. The integrated circuit according to claim 1, wherein said first and second interconnects are disposed in an at least partly overlapping manner as seen in a direction of a normal to said substrate, said normal being disposed perpendicular to said substrate surface.

3. The integrated circuit according to claim 1, wherein:

said second interconnect has:

a first section connected to said second connecting element and running in said first wiring plane; and

a second section running in said second wiring plane; and

a contact connects said first and second sections of said second interconnect to one another, said contact running from said first wiring plane to said second wiring plane.

4. The integrated circuit according to claim 2, wherein:

said second interconnect has:

a first section connected to said second connecting element and running in said first wiring plane; and

a second section running in said second wiring plane; and

a contact connects said first and second sections of said second interconnect to one another, said contact running from said first wiring plane to said second wiring plane.

5. The integrated circuit according to claim 3, further comprising an insulation layer isolating said first and second wiring planes from one another, said contact being led through said insulation layer substantially in a direction running vertically with respect to said substrate surface.

6. The integrated circuit according to claim 4, further comprising an insulation layer isolating said first and second wiring planes from one another, said contact being led through

said insulation layer substantially in a direction running vertically with respect to said substrate surface.

7. The integrated circuit according to claim 3, further comprising an insulation layer isolating said first and second wiring planes from one another, said contact being led through said insulation layer substantially in a direction normal to said substrate surface.

8. The integrated circuit according to claim 4, further comprising an insulation layer isolating said first and second wiring planes from one another, said contact being led through said insulation layer substantially in a direction normal to said substrate surface.

9. The integrated circuit according to claim 1, wherein:

a plurality of said electrical connecting elements are disposed next to one another as seen in said second direction;

each of said plurality of electrical connecting elements have first and second leads in a course of said first direction;  
and

said first leads are connected to one another.

10. The integrated circuit according to claim 1, wherein:

a plurality of said electrical connecting elements are disposed next to one another as seen in said second direction;

each of said plurality of electrical connecting elements have first and second leads extending in said first direction; and

said first leads are connected to one another.

11. The integrated circuit according to claim 1, further comprising other connecting elements each respectively disposed at least at said first distance from one another, said other connecting elements being disposed next to said first and second electrical connecting elements as seen in said second direction.